REMARKS

The claims are claims 2 and 3.

Figure 3 of the drawings have been amended to correspond to subject matter disclosed in the text.

Claim 2 has been amended to correspond to the subject matter disclosed in the text and to respond to rejections under 35 U.S.C. 112.

Figure 3 has been amended. The connection of sampling clock 70 and leading clock 72 from VCO/INTEGRATOR 38 to DATA RECOVERY 40 is described in the application at page 10, line 33 to page 11, line 9. The single signal line between DATA RECOVERY 40 and PHASE SELECT CIRCUIT/FILTER 42 is described in the application at page 11, line 31 to page 16, line 15 and illustrated in Figures 8 to 11. Note that Figure 11 illustrates the signal EARLYB as an output of DATA RECOVERY 40 and Figure 12 illustrates this signal as an input to PHASE SELECT CIRCUIT/FILTER 42. The connection of PHCODE 82 and PHMUX between PHASE SELECT CIRCUIT/FILTER 42 and PHASE INTERPOLATOR 44 is described in the application at page 17, lines 7 to 10, page 19, lines 32 to page 20, line 6 and page 20, lines 19 to 29. The connection of 8 clock signals from VCO/INTEGRATOR 38 to PHASE INTERPOLATOR 44 is described in the application at page 20, lines 7 to 11. The clock signals are denoted ck0, ck1, ck2, ck3, ck4, ck5, ck6 and ck7 in Figure 16. The Applicant respectfully submits that by these amendments the drawings now properly illustrate all limitations of the current claims.

Claims 2 and 3 were rejected under 35 U.S.C. 112, second paragraph, as failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 2 as amended is proper under 35 U.S.C. 112. Regarding the reference to "said clock output of said voltage controlled oscillator" the paragraph reciting the voltage controlled

oscillator now recites "plural outputs each generating a corresponding clock signal at differing phases." This provides antecedent basis for later recitations of "plural clock signals at differing phases of said voltage controlled oscillator."

Reference to "phase interpreter" has been amended to "phase interpolator" as taught in the application.

Regarding the reference to "said data recovery error signals" in lines 23 and 28 of claim 2, this language has been deleted. This term has been replaced with "early/late signal." Claim 2 has been amended to state that this early/late signal is generated by the data recovery block. Production of the early/late signal by DATA RECOVERY 40 is described in the application at page 11, line 31 to page 16, line 15 and illustrated in Figures 8 to 11. Figure 11 illustrates the signal EARLYB as an output of DATA RECOVERY 40 and Figure 12 illustrates this signal as an input to PHASE SELECT CIRCUIT/FILTER 42. Accordingly, the new language is believed proper under 35 U.S.C. 112.

Regarding the term "said two clock outputs of said phase selection circuit" in line 25 of claim 2, this recitation has been amended to "interpolation code" and "phase select code." Generation of these two signals by PAHSE SELECT CIRCUIT/FILTER 42 is described in the application at page 16, line 26 to page 19, line 23. This portion of the application includes description of PHCODE 82 at page 17, lines 7 to 9 and PHMUX at page 17, lines 9 and 10. Accordingly, the new language is believed proper under 35 U.S.C. 112.

The Applicant submits that the subject matter of amended claim 2 is adequately described in the original application. Generation of plural clock signals by VCO/INTEGRATOR 38 is described in the application at page 9, line 25 to page 10, line and illustrated in Figure 3. The sampling clock and leading clock are described in the application at page 10, line 33 to page 11, line 9. The

sampling by the sampling clock and the leading clock is described in the application at page 11, lines 14 to 16. The production of the early/late signal is described in the application at page 11, line 31 to page 16, line 15 and illustrated in Figures 8 to 11. The claimed early/late signal corresponds to EARLYB illustrated in Figures 11 and 12. The application describes the operation of the phase selection circuit at page 16, line 26 to page 19, line 23 and illustrates this in Figure 12. The application describes the interpolation code as thermometer code 82 at page 17, lines 7 to 9. The application described the phase select code at page 17, lines 9 to 10. The operation of the phase interpolator is described in the application at page 19, line 24 to page 20, line 29 and is illustrated in Figure 16. Receipt of the plural clock signals of differing phases is described in the application at page 20, lines 7 to 9. The interpolation code is "thermometer code ic(0:15) and ic_b(0:15) 82" noted in the application at page 20, lines 1 to 2 and lines 27 to 29. The reference number 82 corresponds to PHCODE 82 described in the application at page 17, lines 7 to 9 and illustrated in Figure 12. The phase select code is "control signals sE0, sE1, sO0 sO1, invE, invE_b, invO and invO_b" which are described in the application at page 20, lines 19 to 21 as produced by phase select logic 42 and used to select clock vectors. The selection of two adjacent phases for interpolation is described in the application at page 20, lines 9 to 12.

The Applicants respectfully request entry and consideration of this amendment. Entry of this amendment is proper at this time because the amendment serves only to clarify subject matter previously recited. Thus no new search or reconsideration is required.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early

entry of this amendment, reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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Respectfully submitted,

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